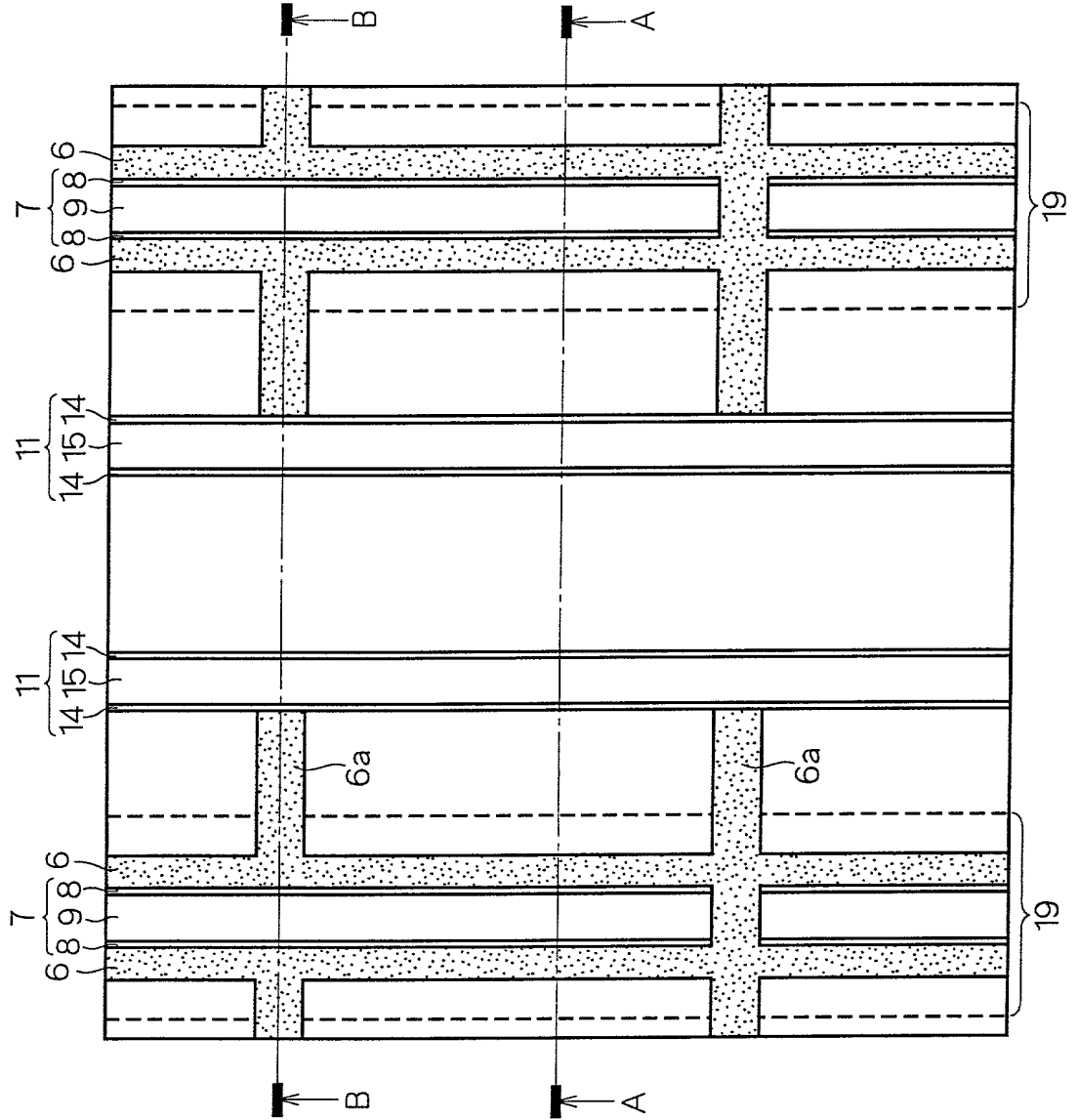


[illegible]

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INV: Hideki TAKAHASHI
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Figure 1 is a cross-sectional view of a semiconductor device. The device consists of a substrate with a P+ region (1) and an N- region (3). A series of vertical structures are formed on the surface, including a central P region (15) and two N+ regions (5) on either side. The structures are labeled with numbers 1 through 15. A time axis t_0 is indicated at the bottom.

FIG. 3



[illegible]

FIG. 5

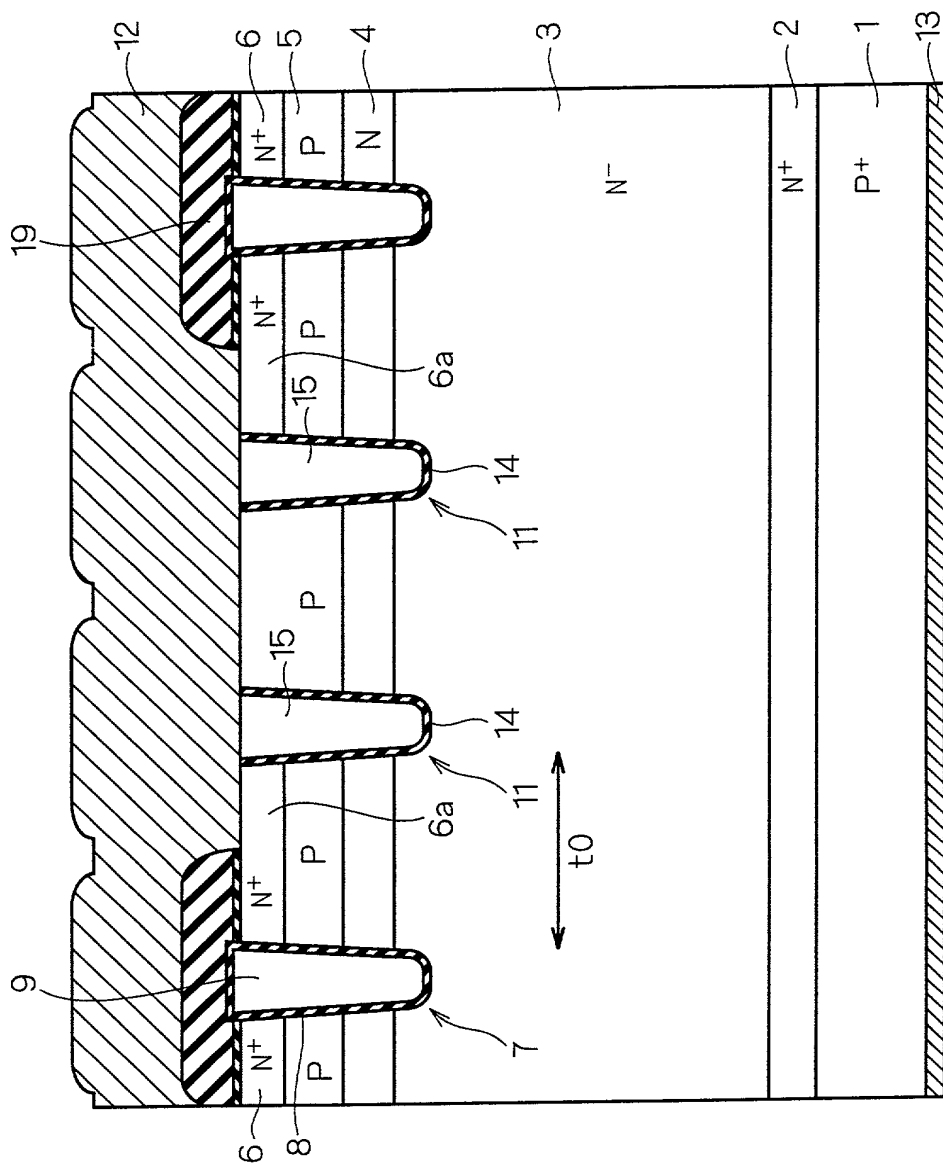


FIG. 6

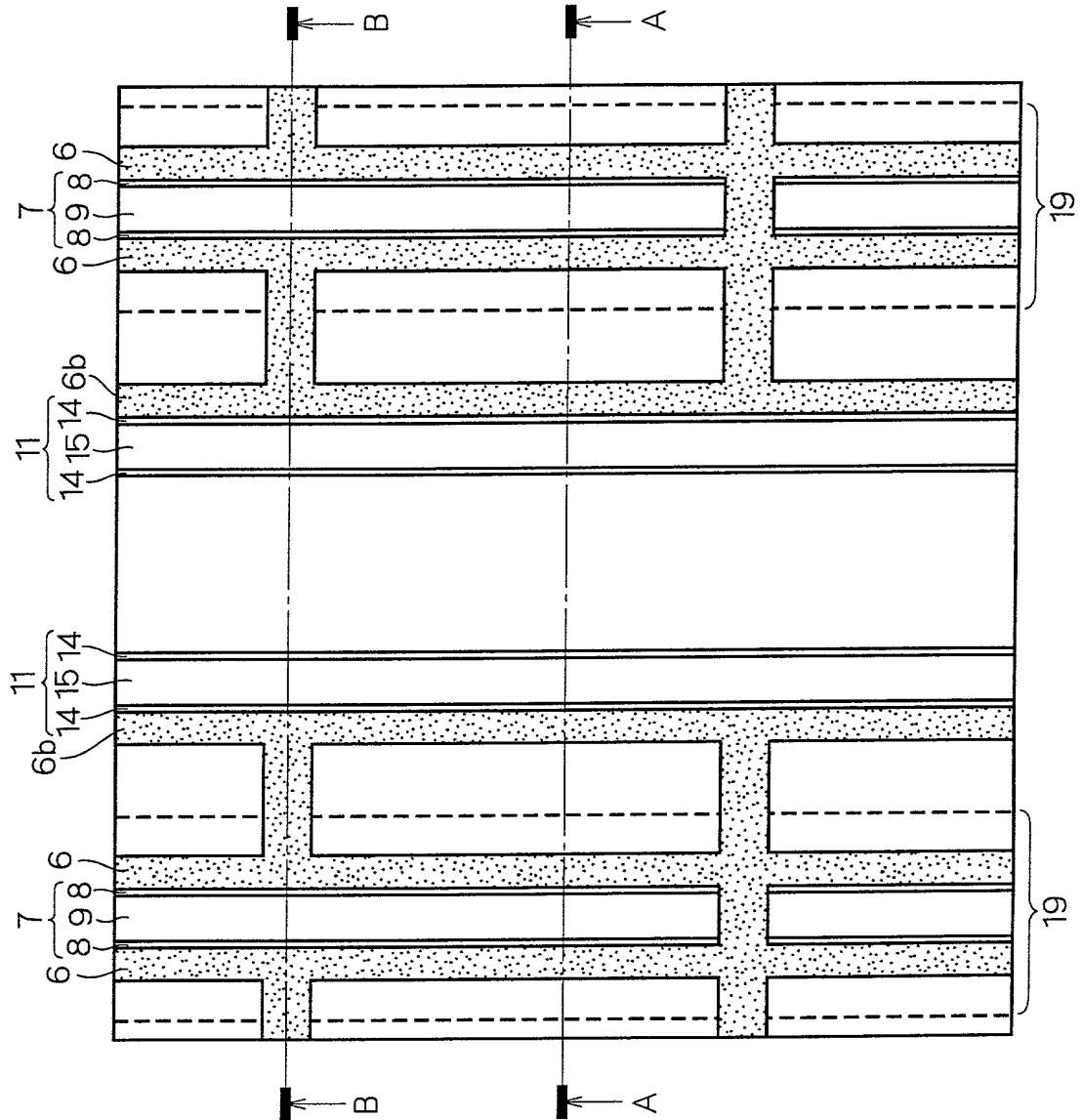


FIG. 7

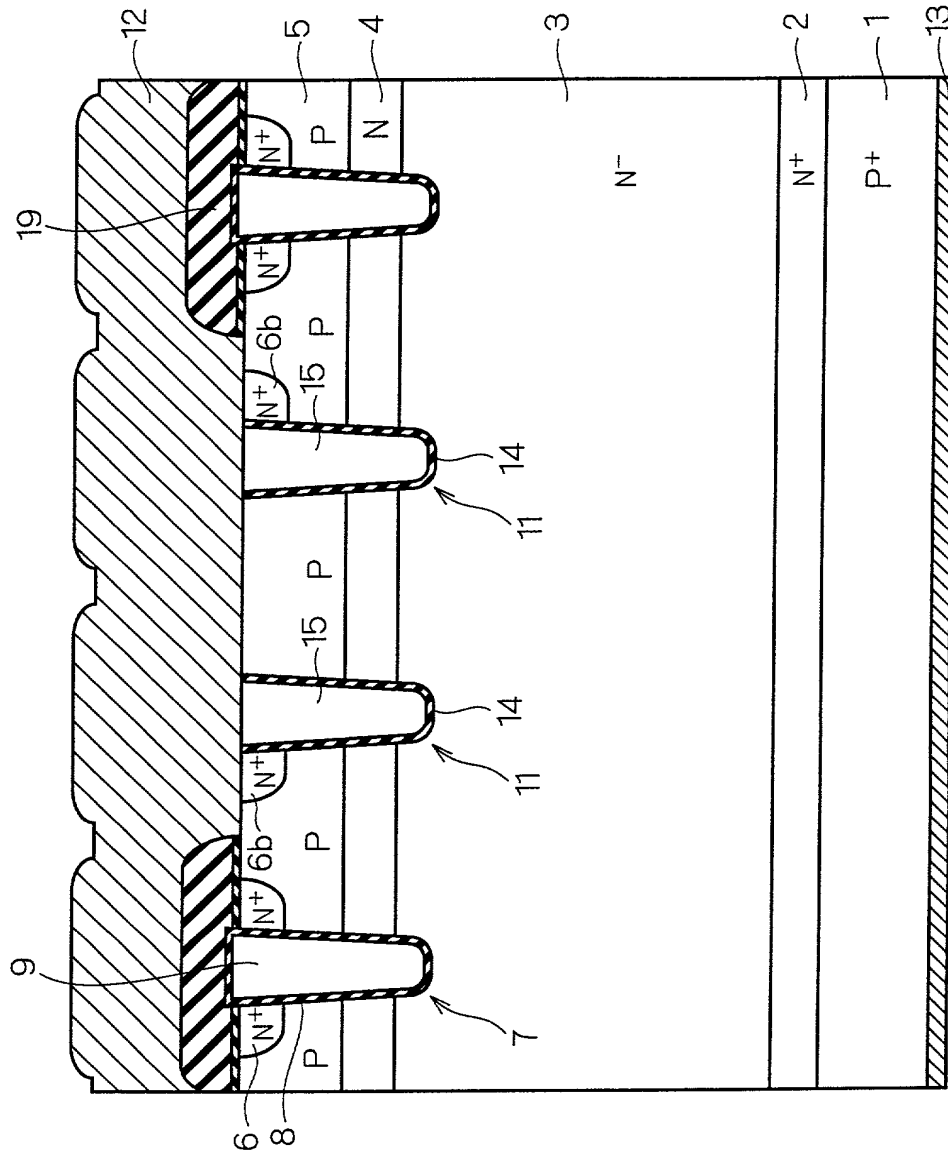


FIG. 8

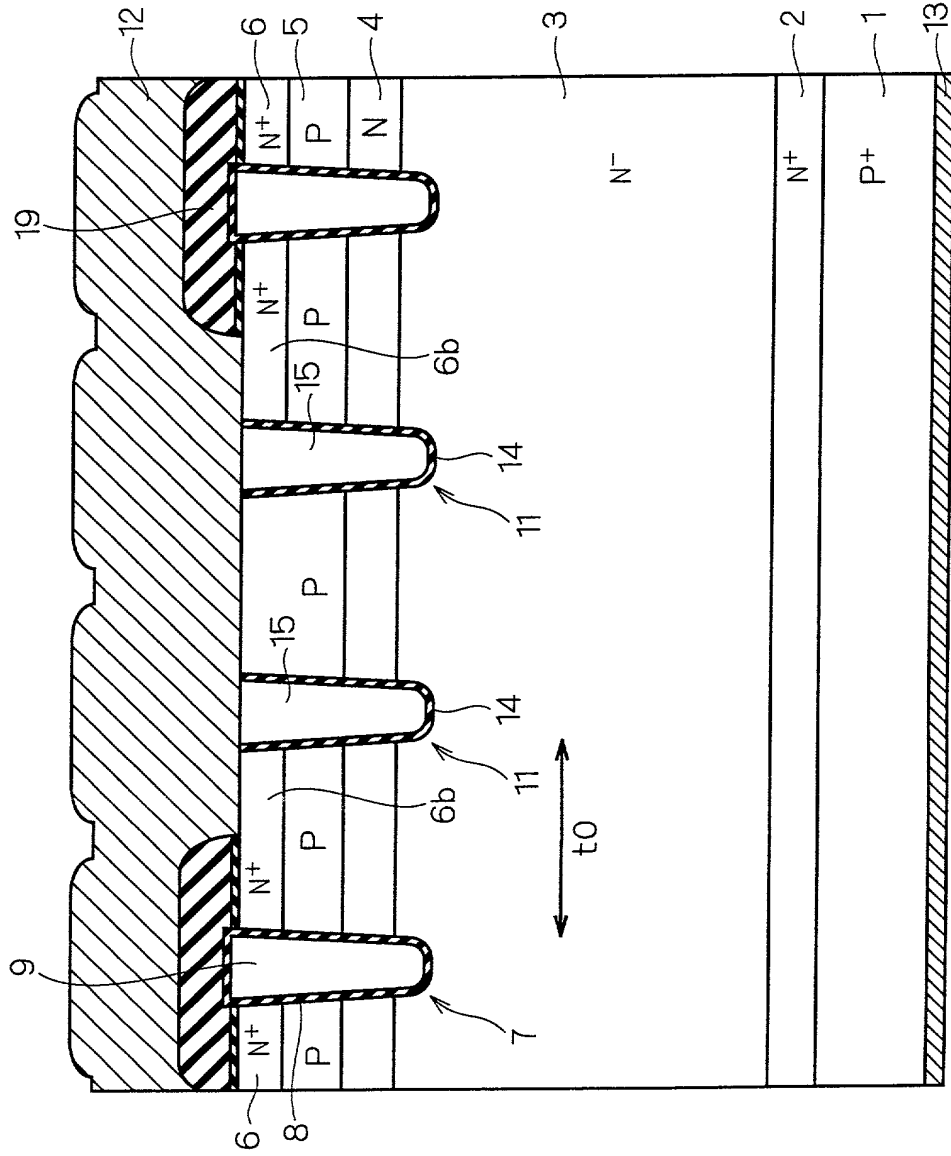


FIG. 9

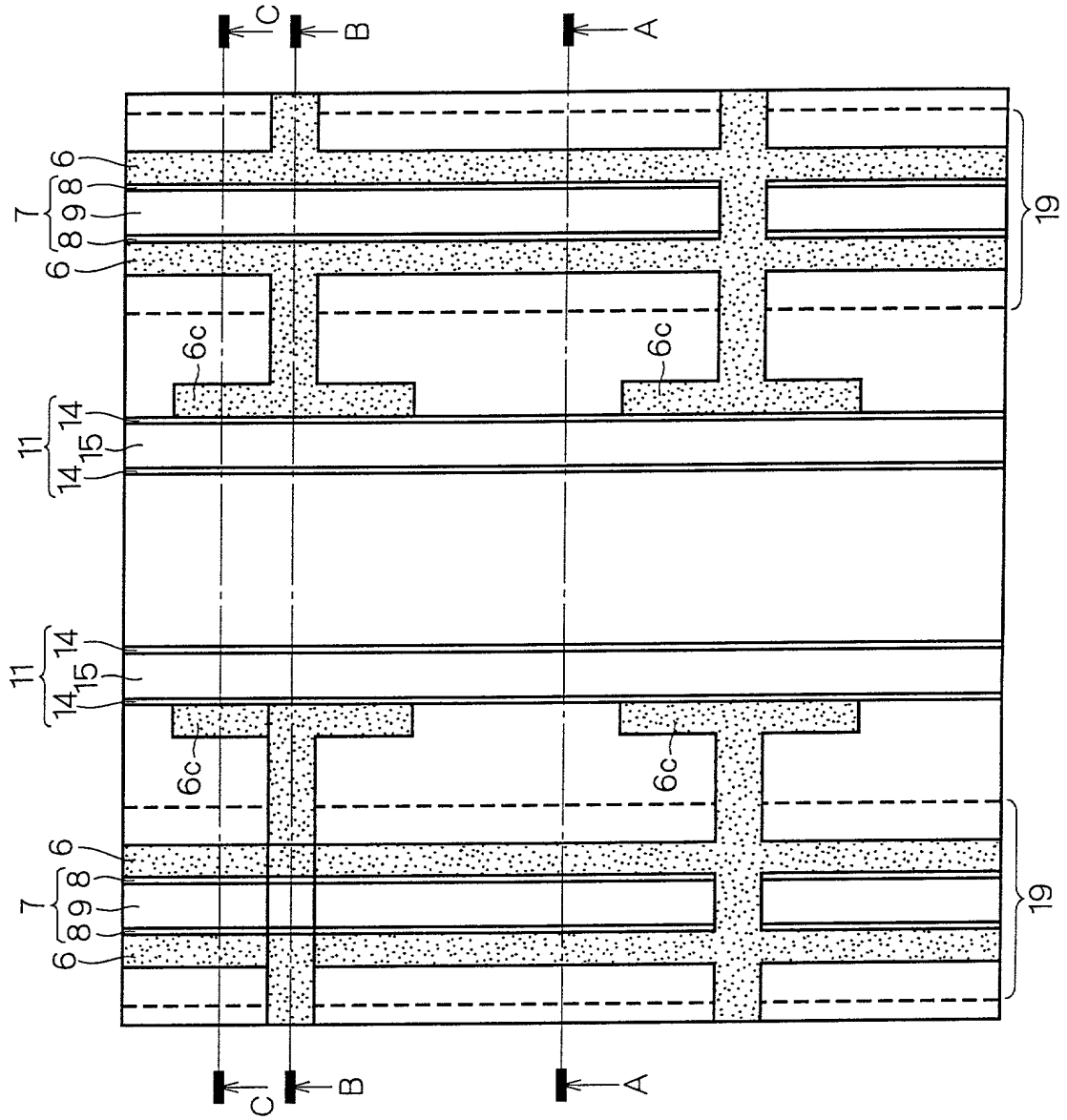
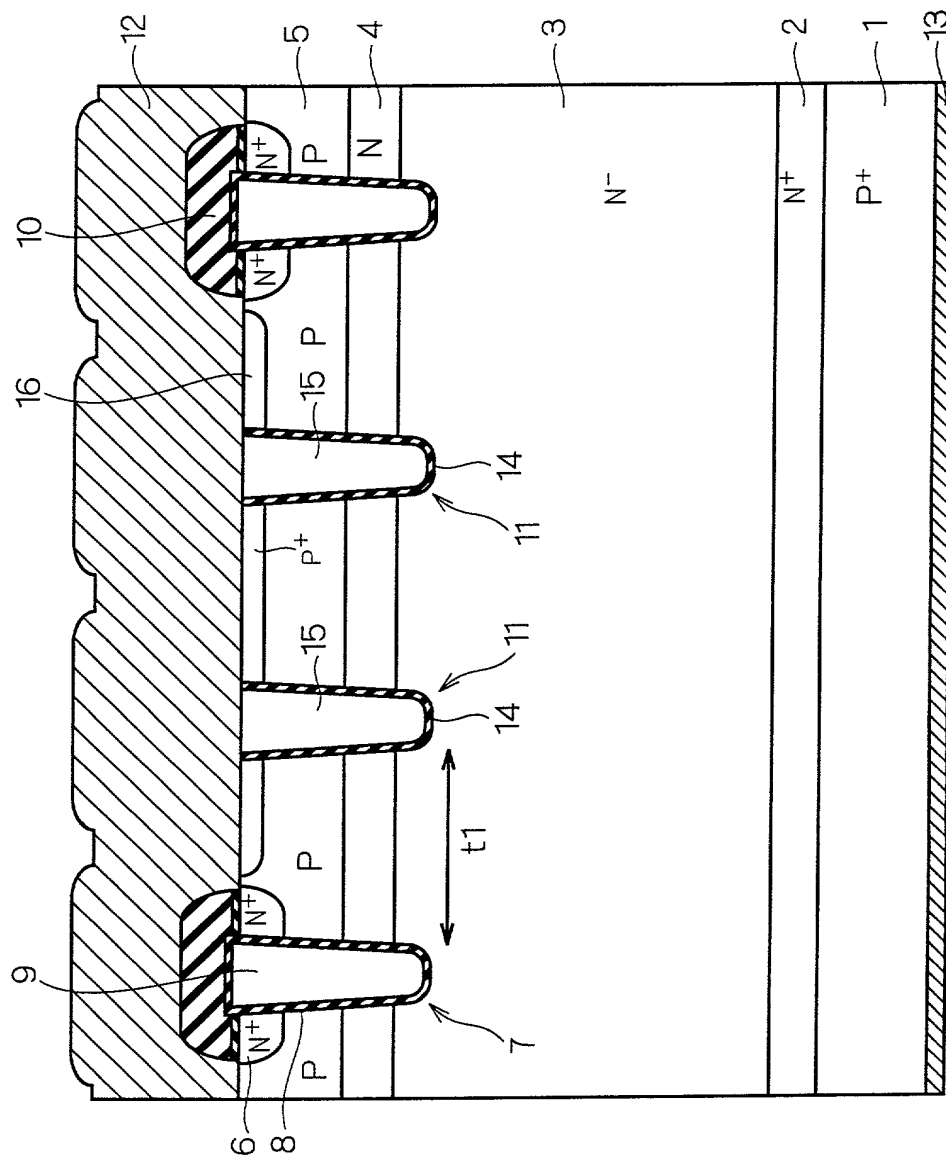


FIG. 9

FIG. 10



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FIG. 11

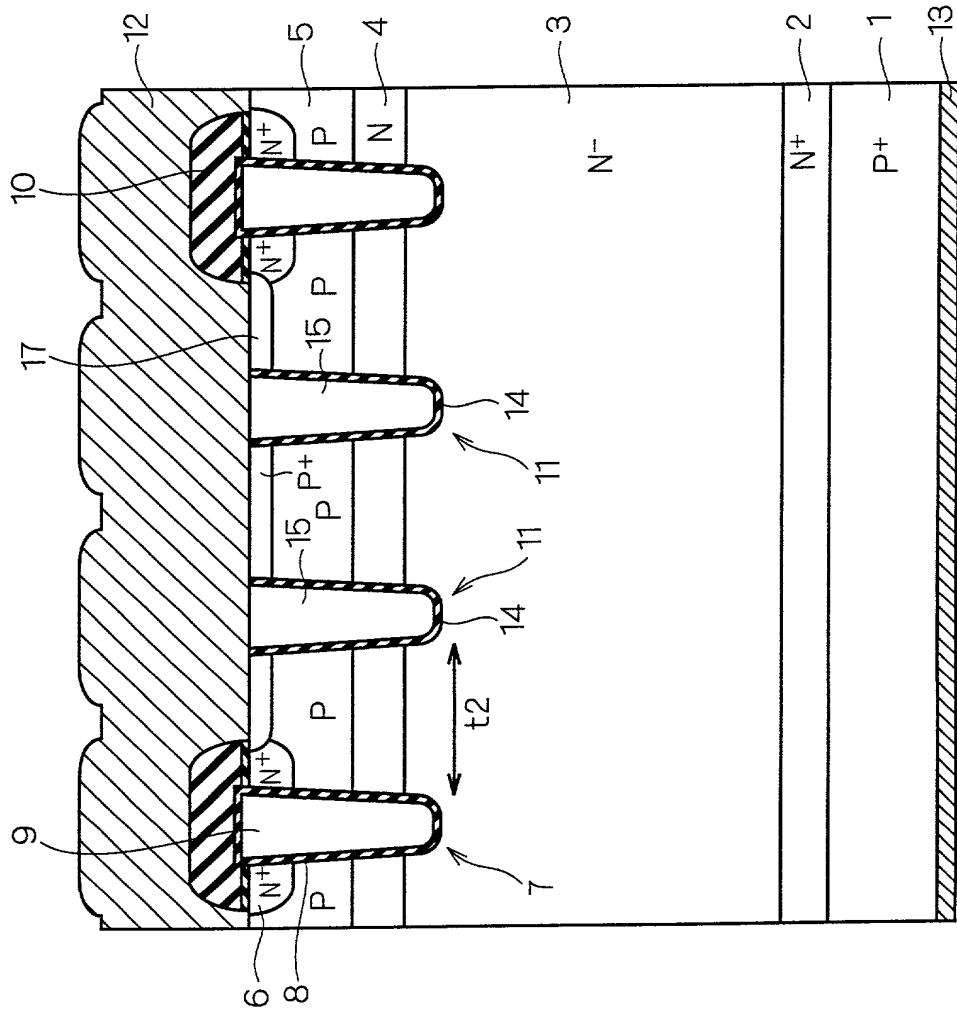
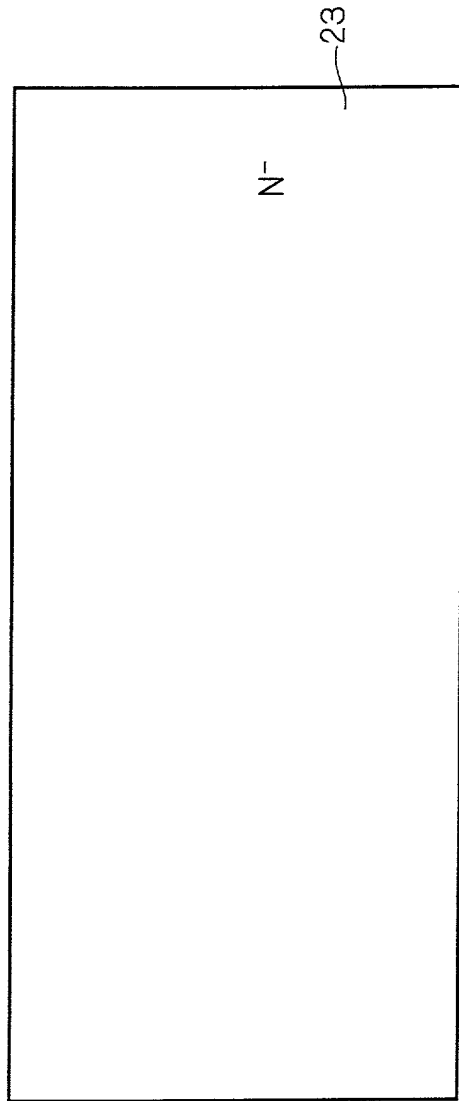


FIG. 11

FIG. 12

FIG. 12



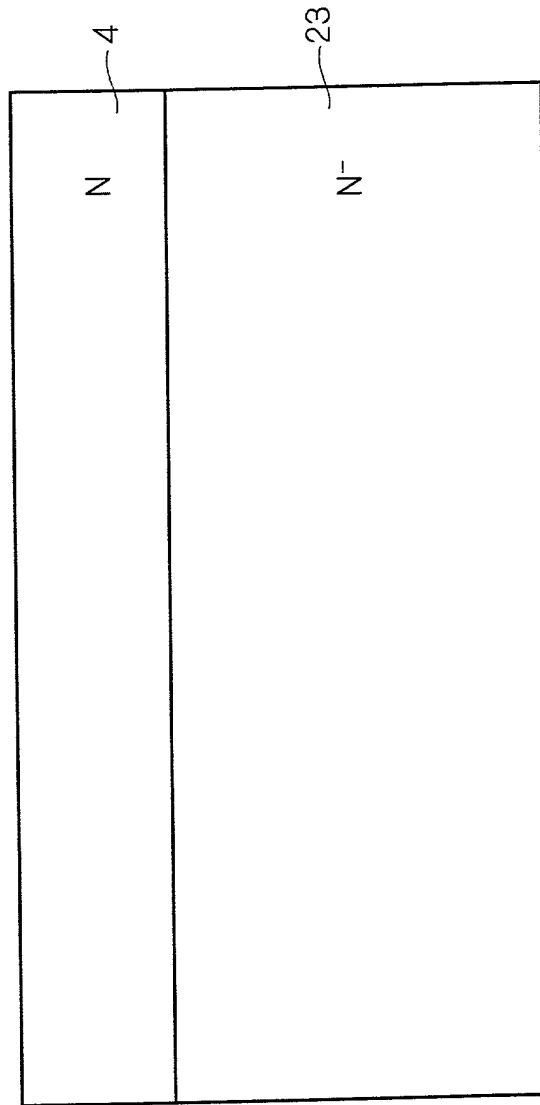


FIG. 13

FIG. 13

FIG. 14

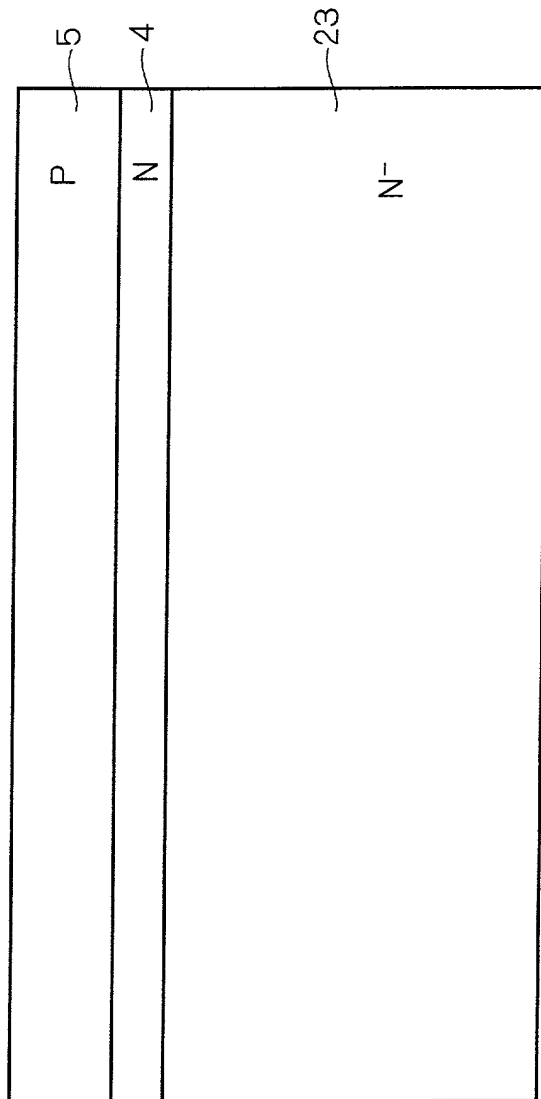


FIG. 15

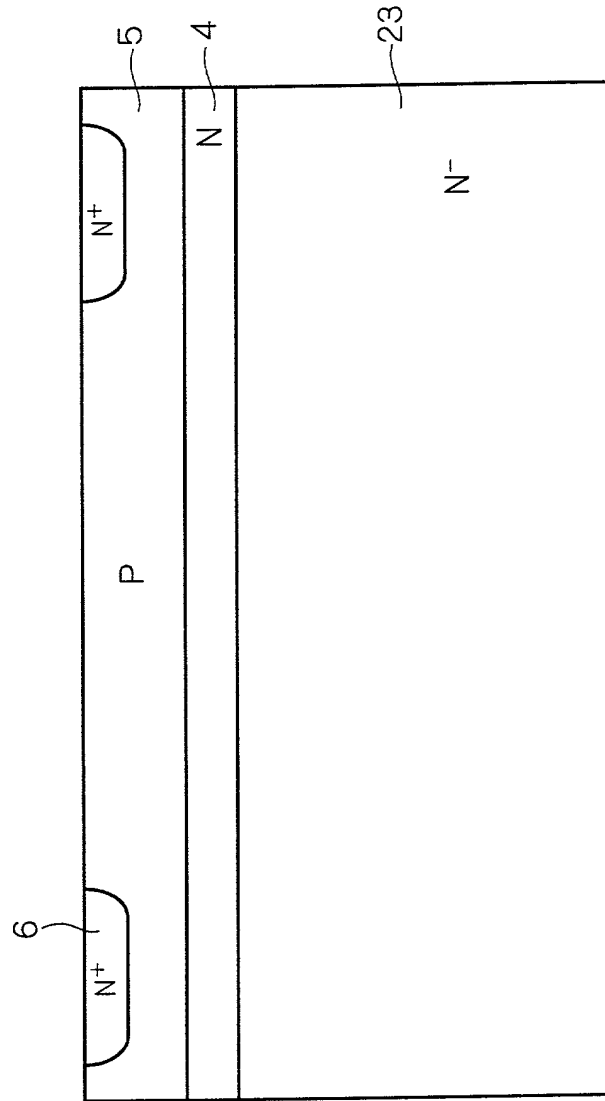


FIG. 16

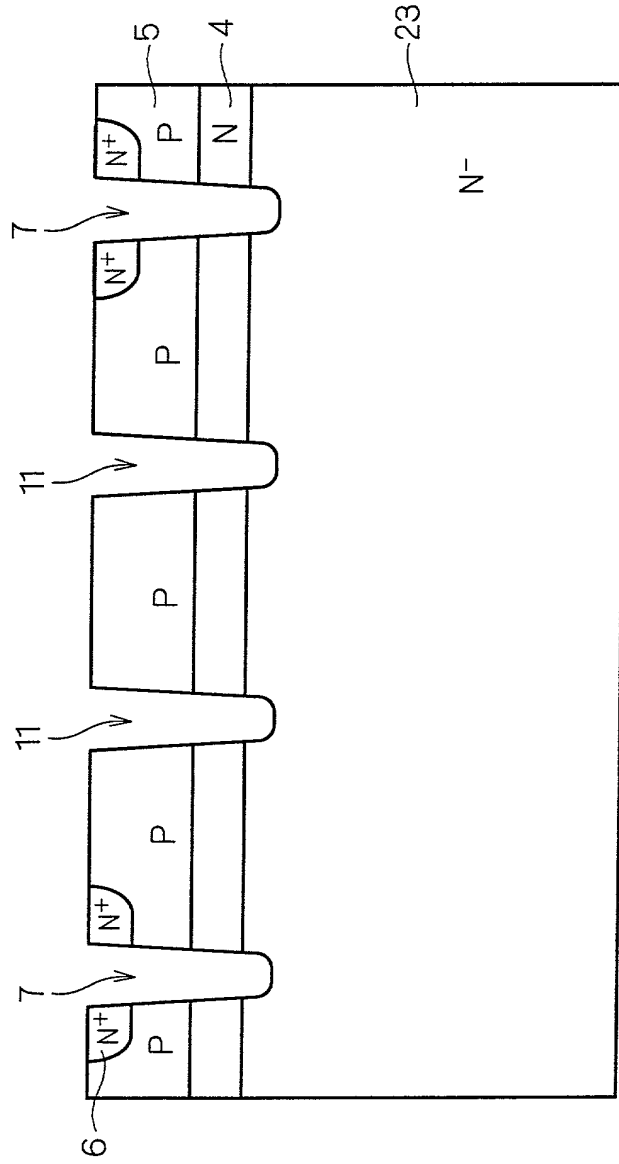


FIG. 17

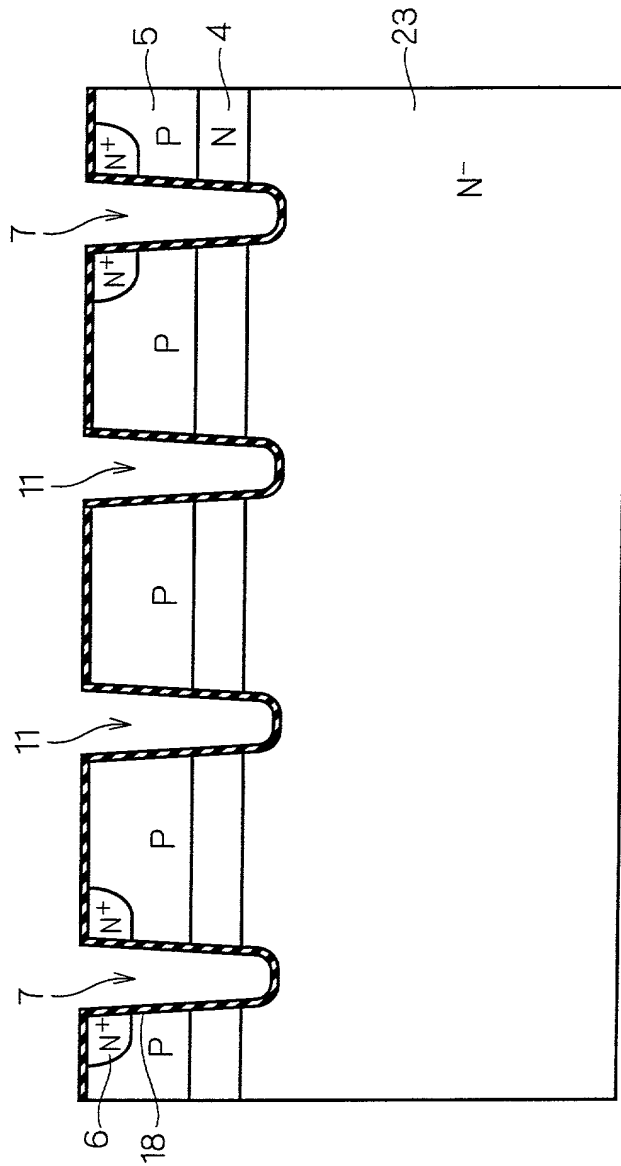


FIG. 17

FIG. 18

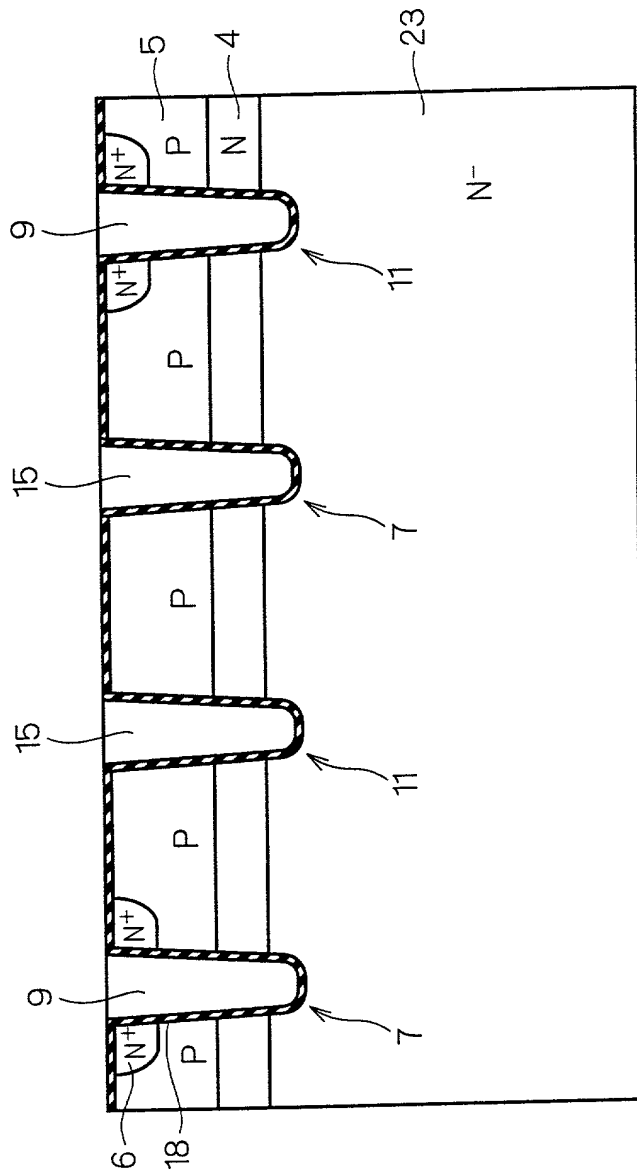
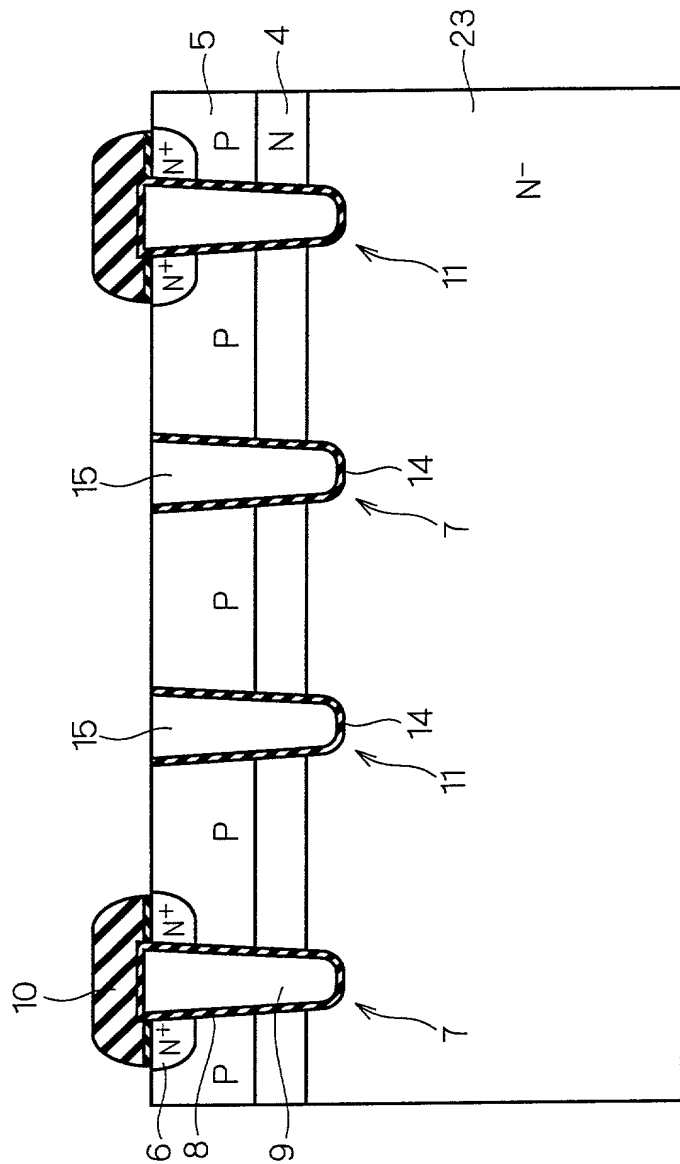


FIG. 19



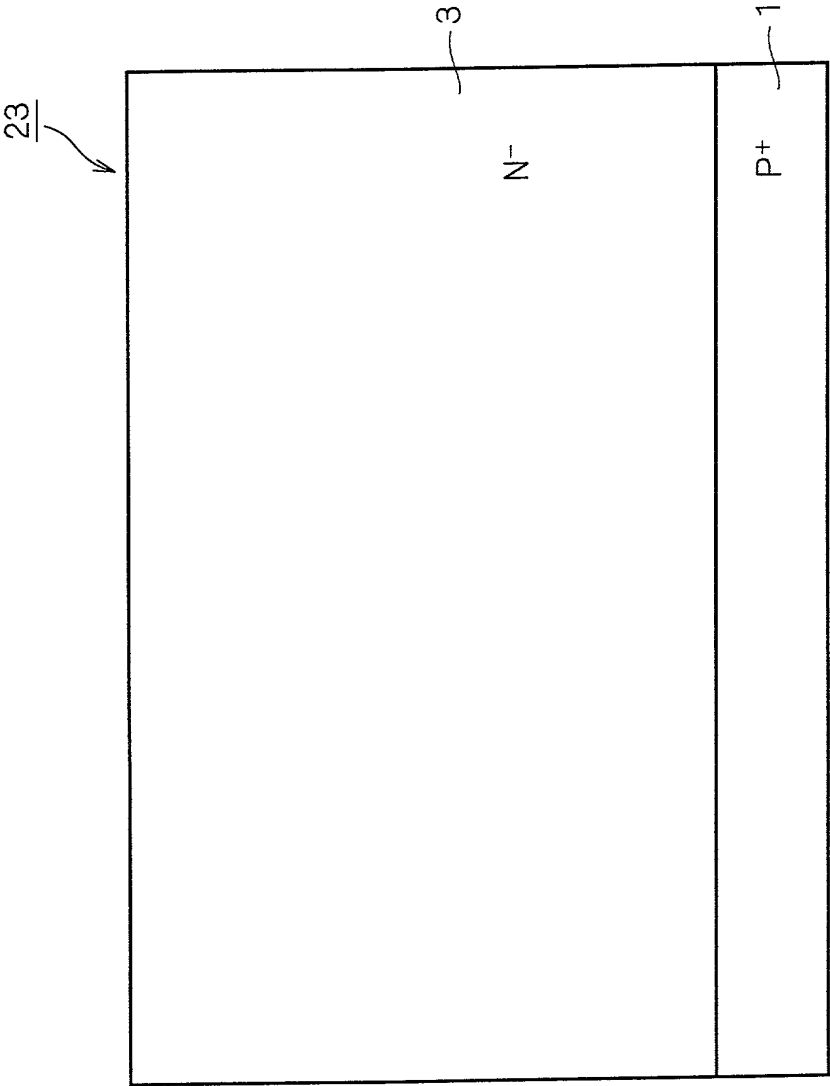
[illegible]

FIG. 21

FIG. 21



FIG. 22



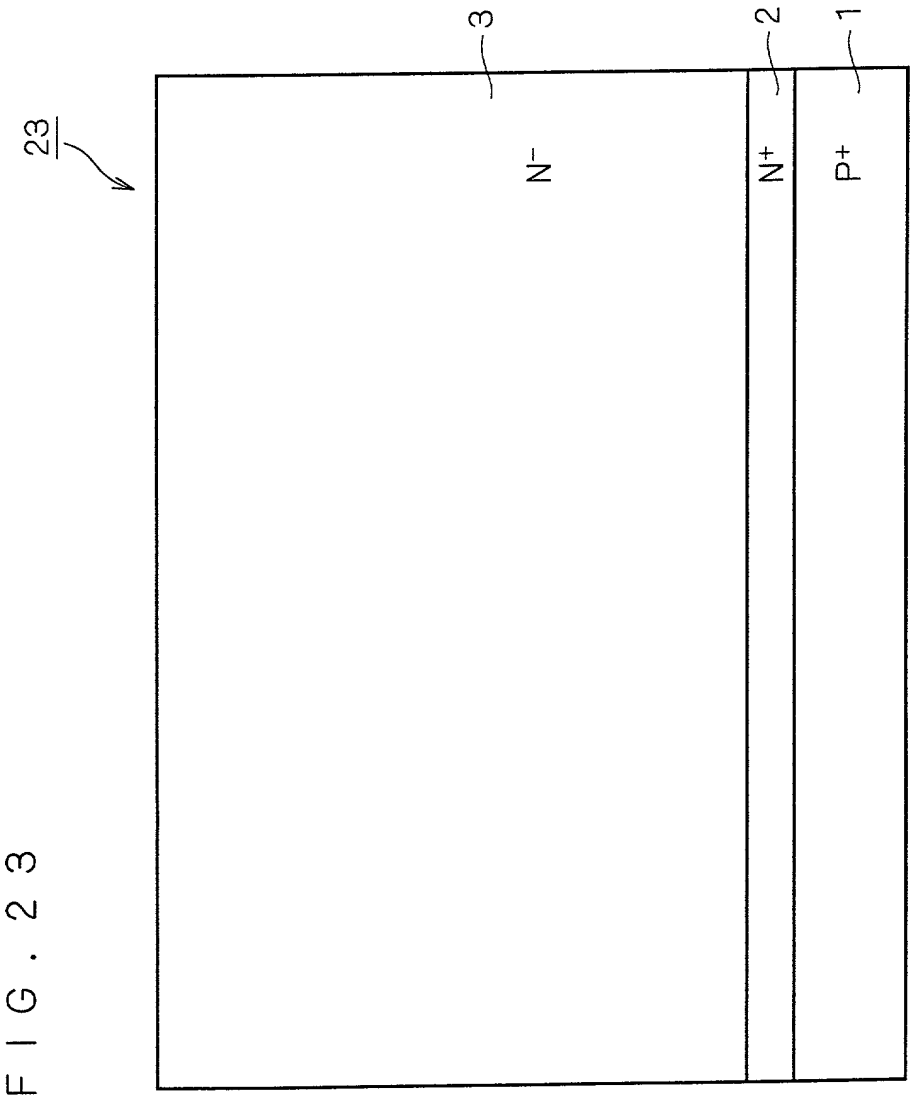
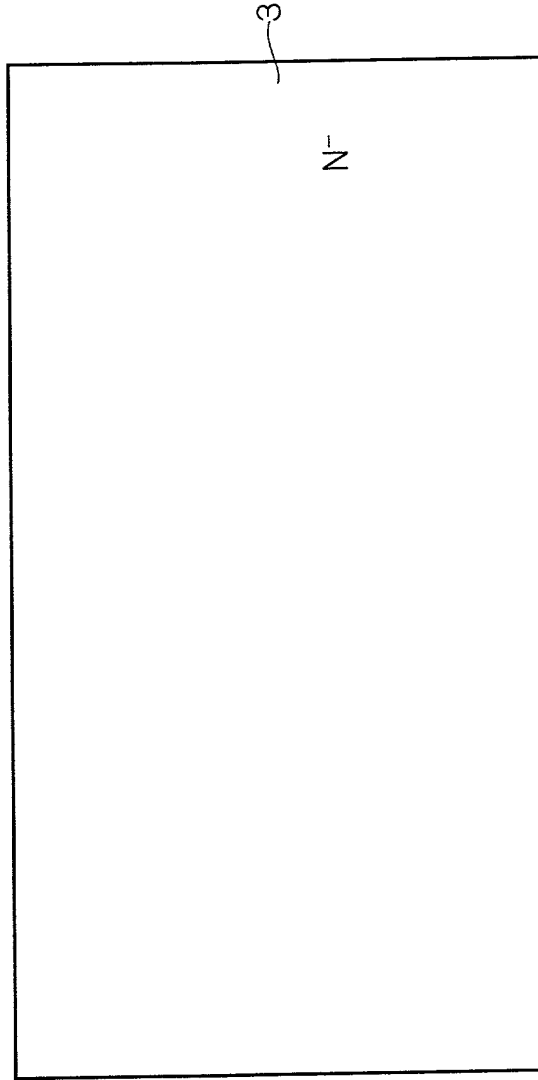


FIG. 24

FIG. 24



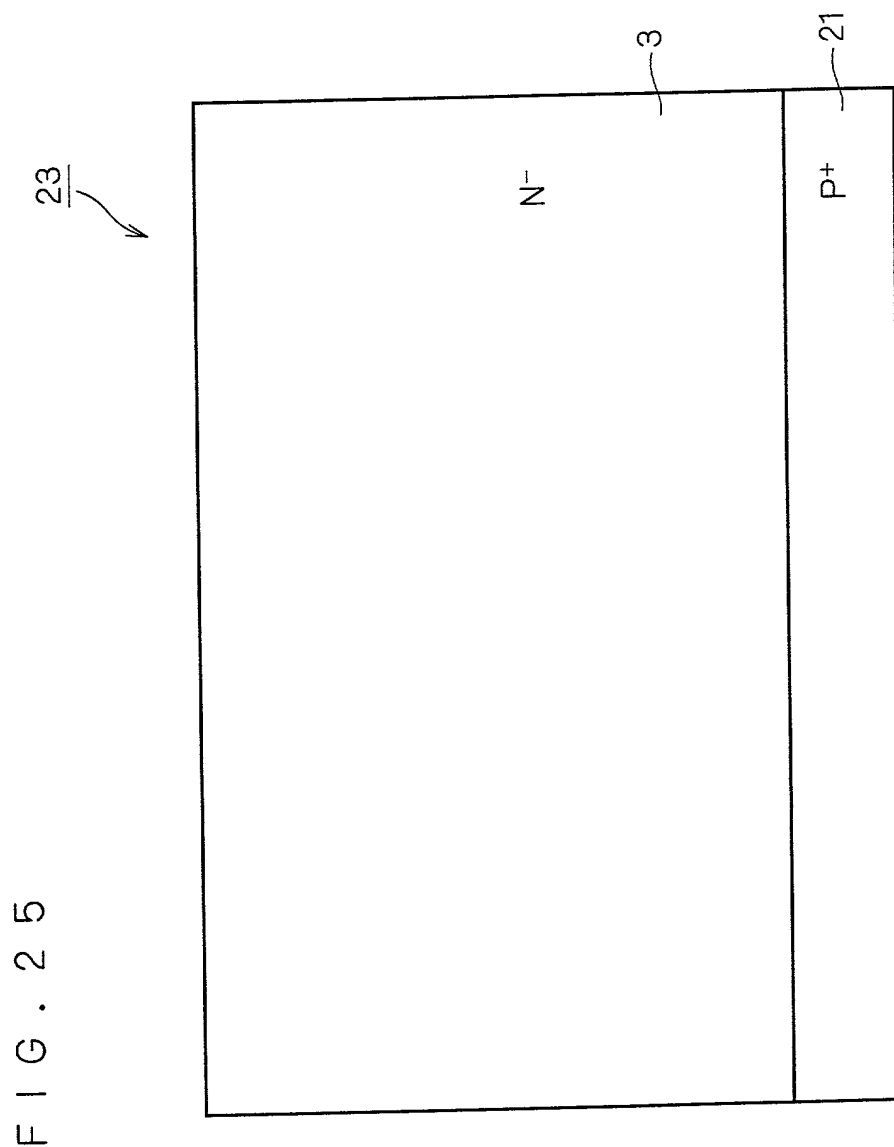
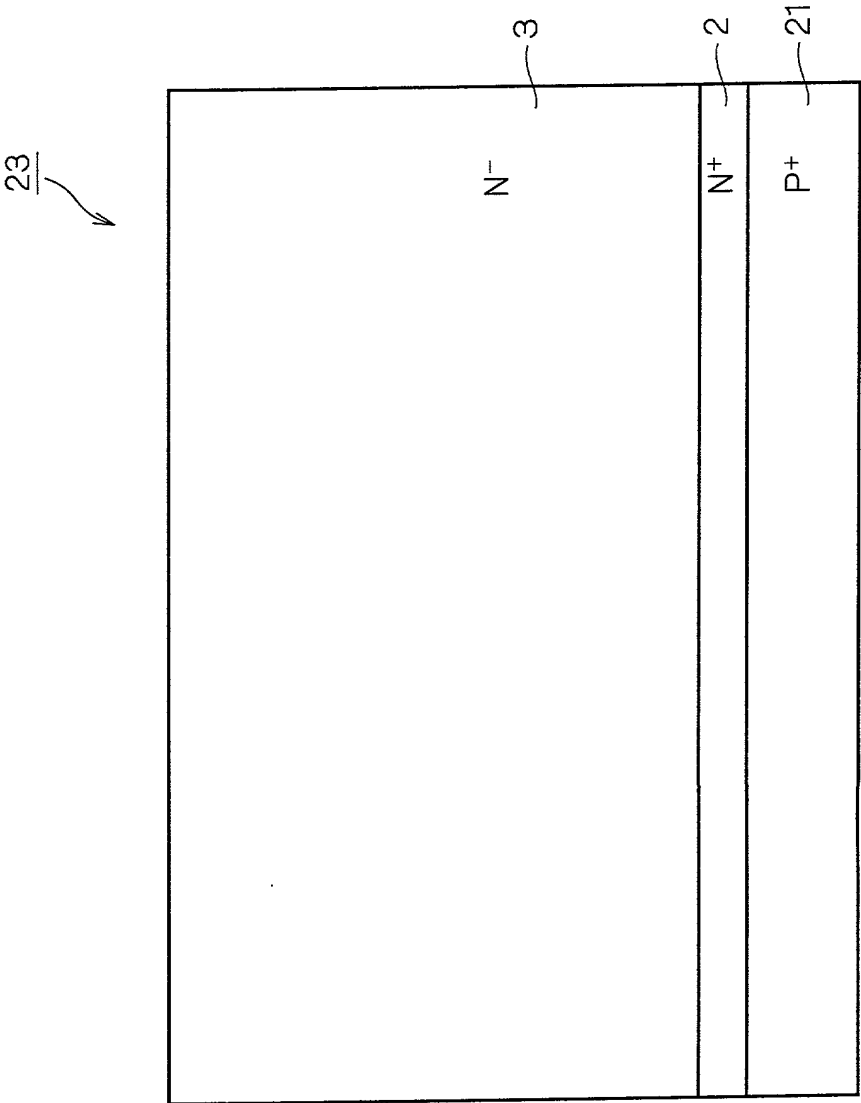


FIG. 26

FIG. 26



This cross-sectional view shows a semiconductor device with a substrate 31 having layers 32, 33, and 34. Four vertical structures 37 are formed on the substrate. Each structure 37 has a base 38 and a top 39. The base 38 is formed in a P region 35, and the top 39 is formed in an N⁺ region 36. The structures 37 are separated by regions 40. The top surface of the device is covered by a layer 42.

FIG. 28

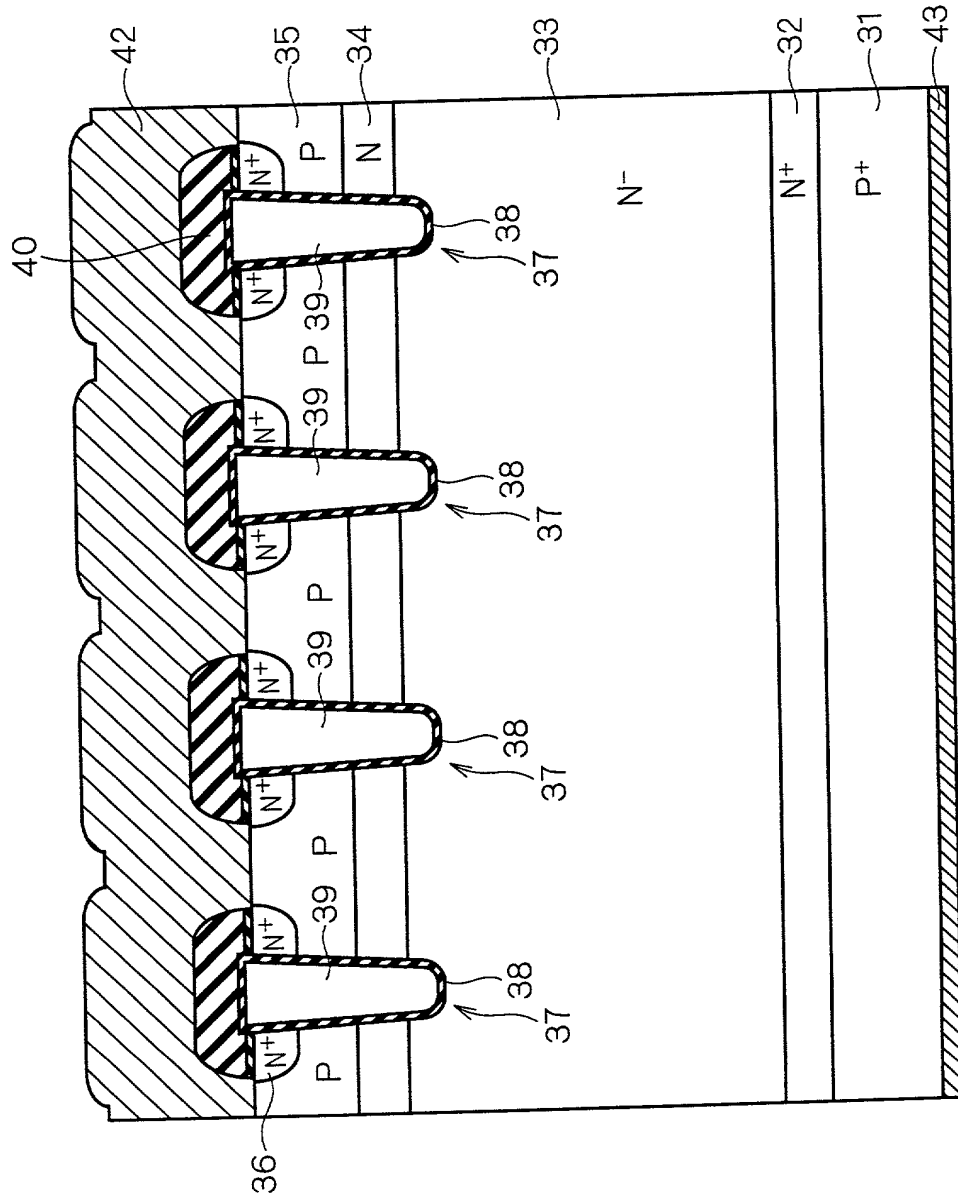
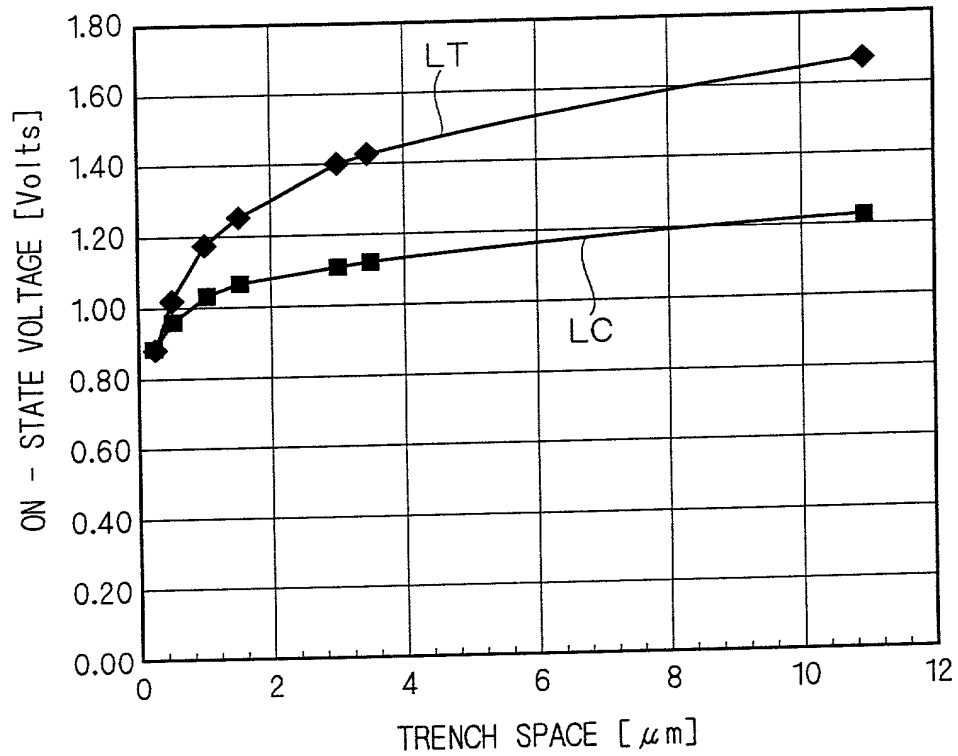


FIG. 29



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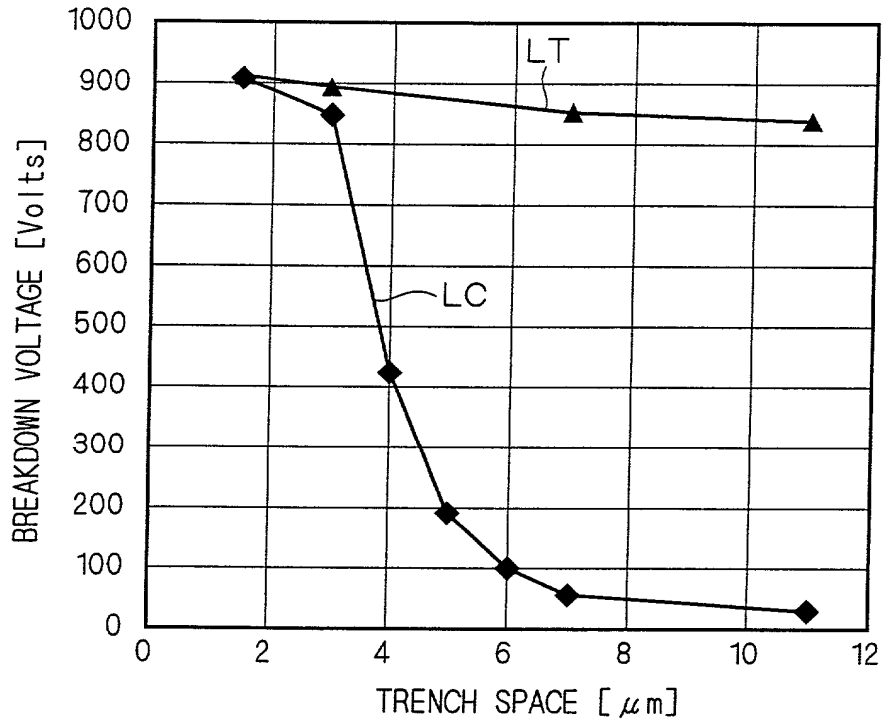


FIG. 31

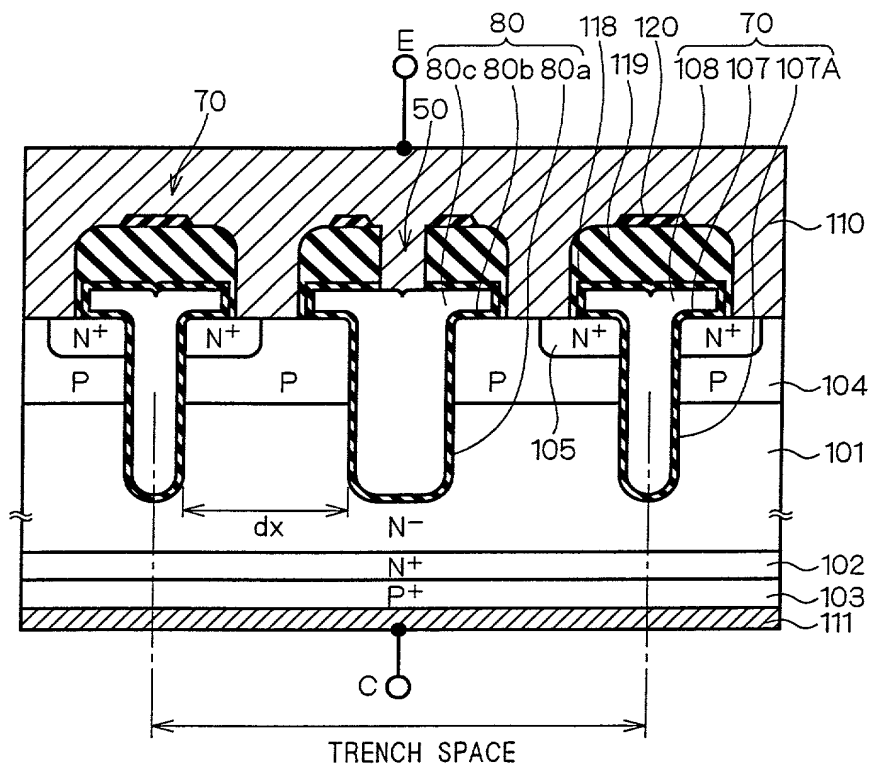


FIG. 32

